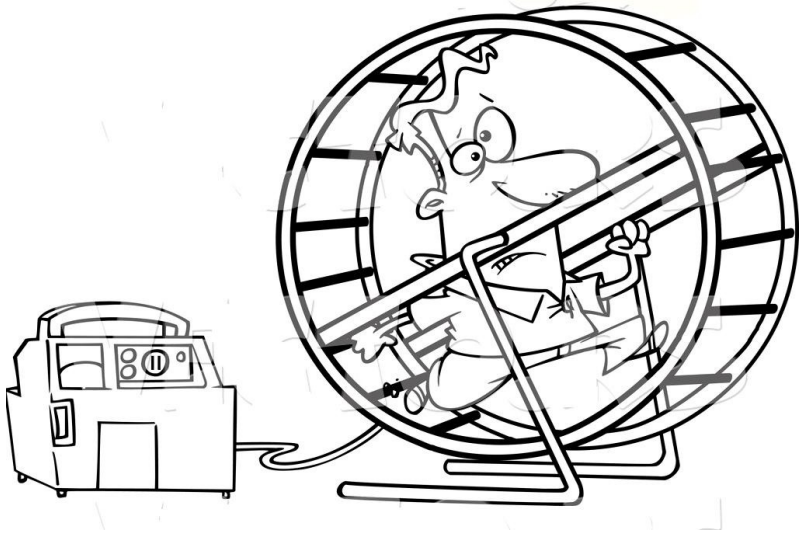
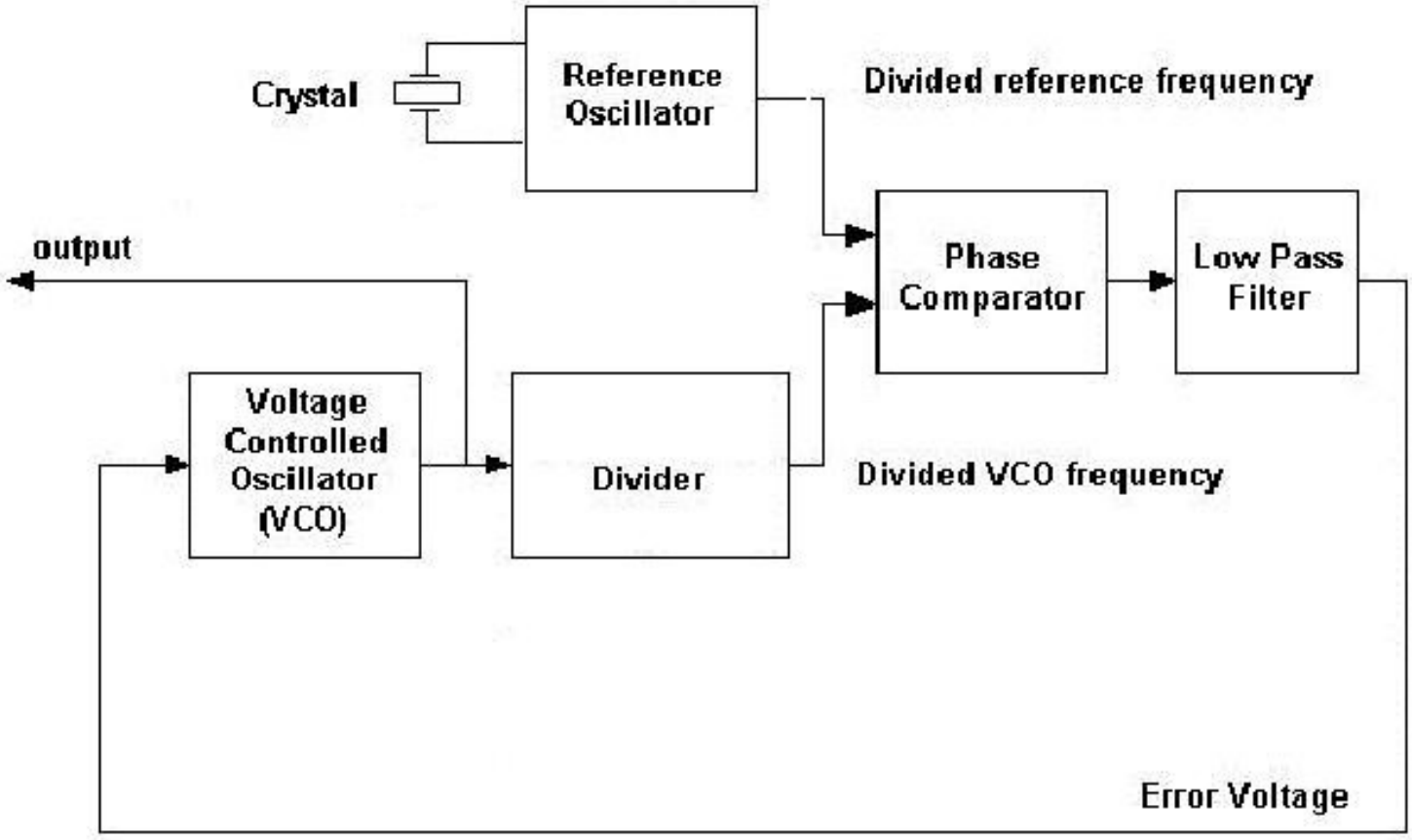
The New England Radio Discussion Society electronics course (Phase 4, cont'd)

Generating RF, Let's Count The Ways ...

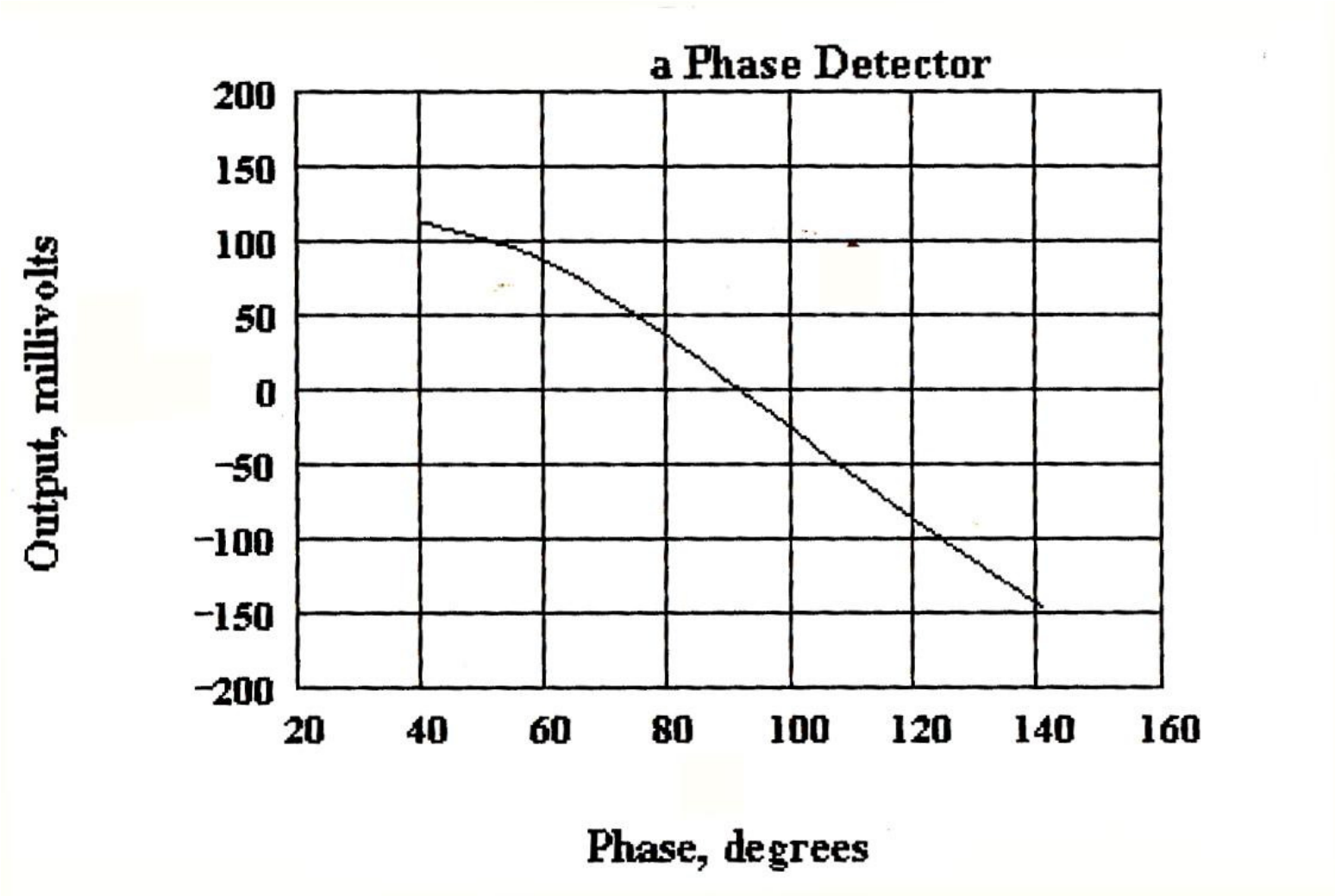


AI2Q – April 2017

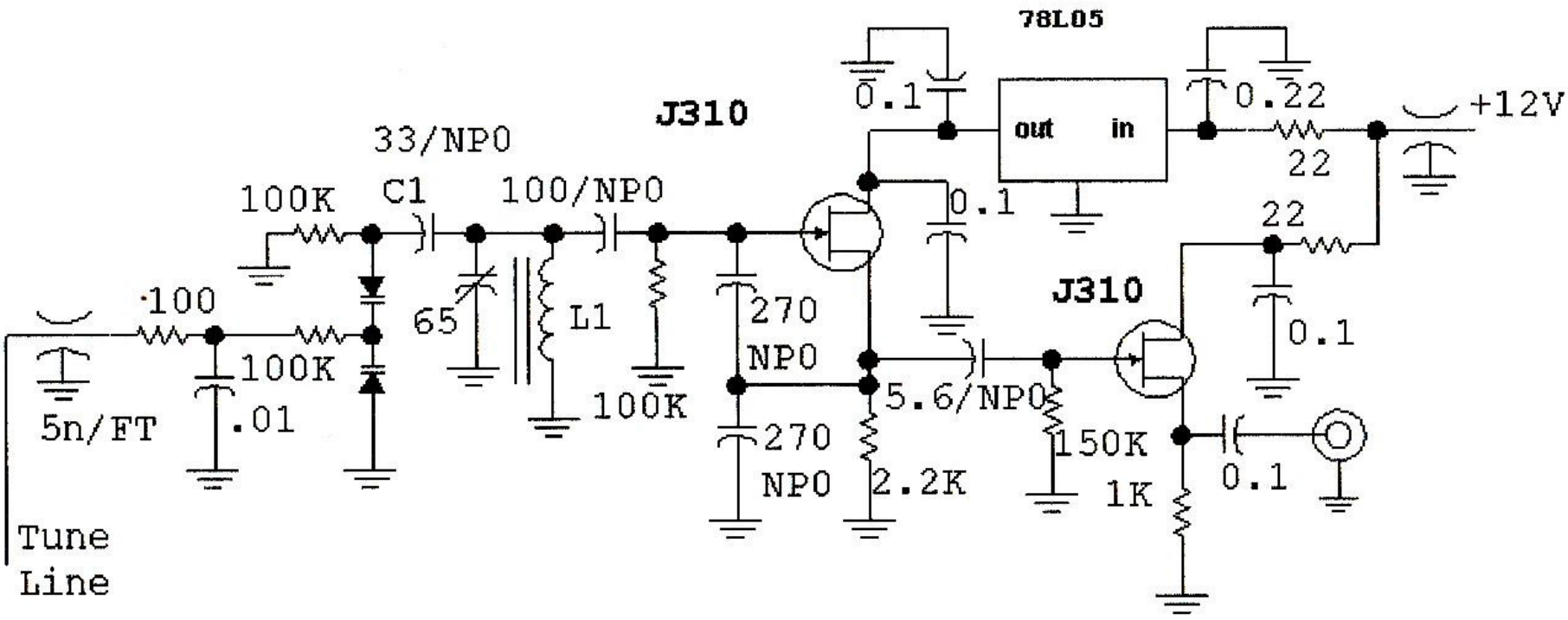
A *phase-locked loop*, or *PLL*, is a negative feedback system where an oscillator is *phase-locked* to a reference signal. It is analogous to a car's cruise control.



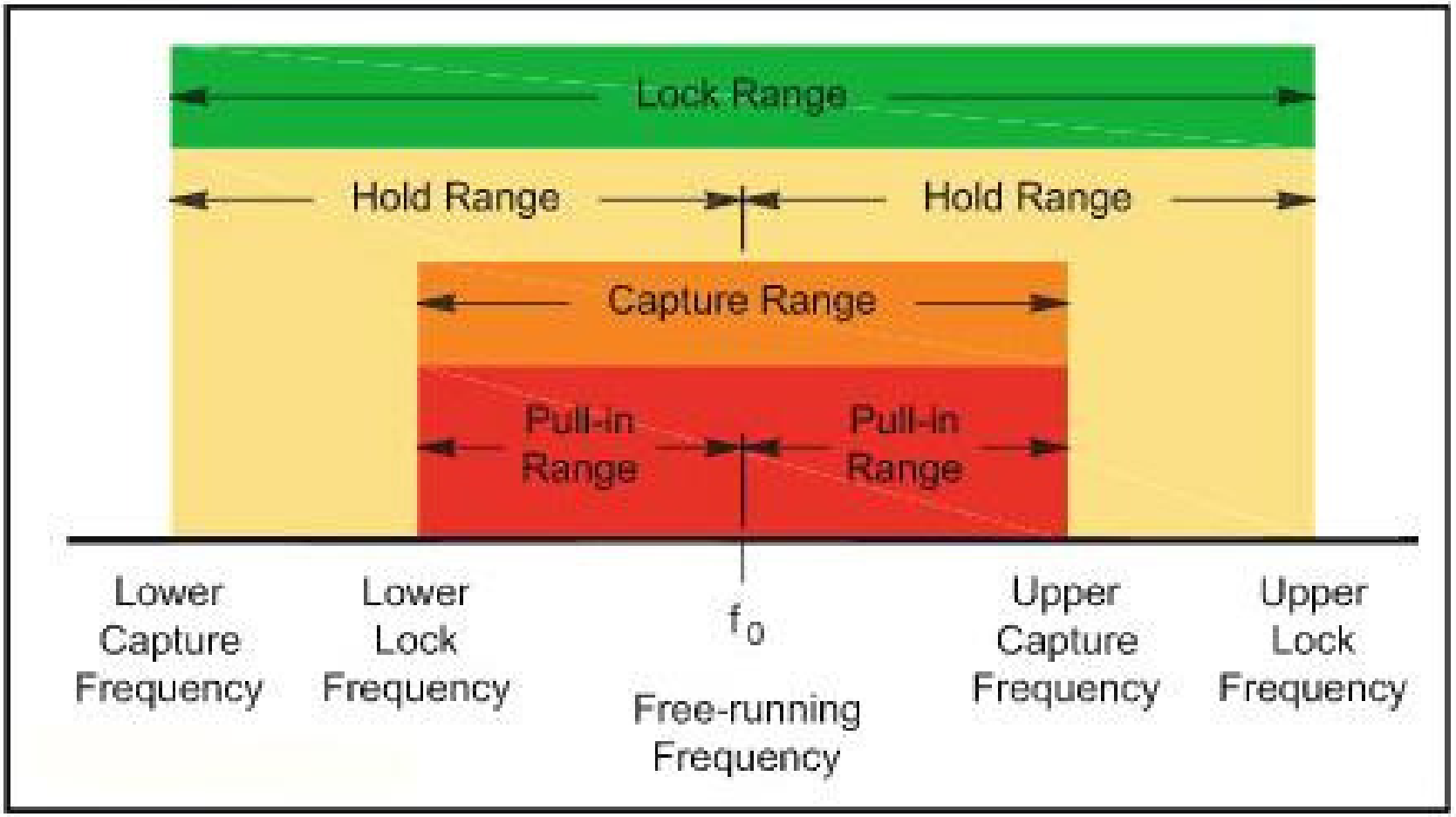
The *phase detector* circuit generates a DC *error voltage* that's proportional to phase/frequency shifts.



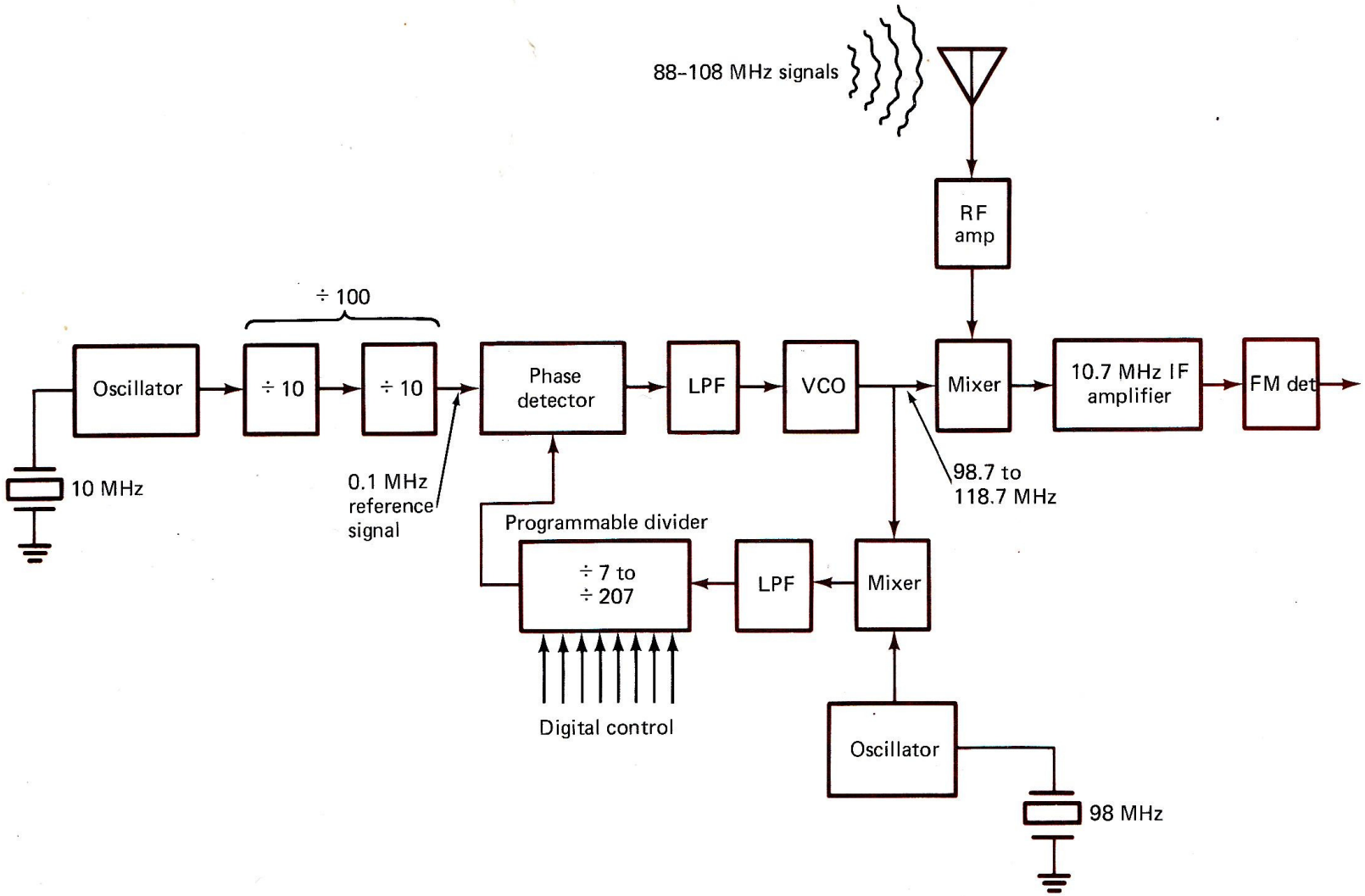
Here's a typical circuit for a VCO and buffer, using JFET devices. This one was used in a synthesizer experiment for the 20 meter band.



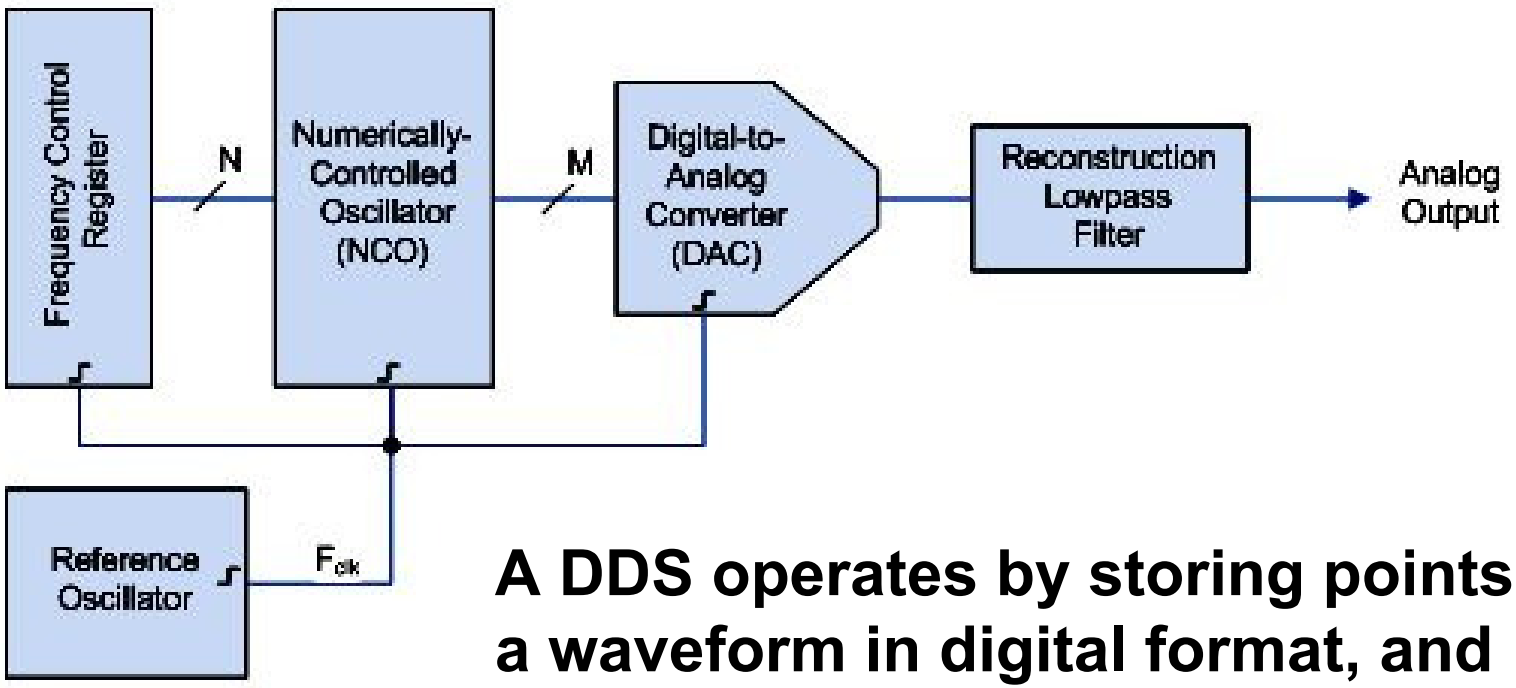
This graph shows how the PLL loop reacts.



This block diagram shows the PLL architecture for a digitally tuned FM broadcast band radio.



Enter the *direct digital synthesizer*, or *DDS*



A DDS operates by storing points of a waveform in digital format, and then recalling them to generate a waveform. The rate at which the synthesizer completes one waveform sets the frequency.

The DDS uses memory to store a number corresponding to the voltage required for each value of waveform. DDSs uses a *look-up table* to generate a sinewave output. Non-volatile memory typically contains a vast number of points on a waveform.

Tuning is accomplished by increasing or decreasing the size of a step between sample points. A large increment at each update means the output goes to full value faster and the frequency is correspondingly high. Smaller increments mean it takes longer to increase the full cycle value and a correspondingly low value of frequency happens.

A 24 bit system provides over 16 million points and gives a frequency resolution of about 0.25 Hz when used with a 5 MHz clock.

Until next time, 73 de AI2Q